The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GUY L. STEELE JR.

Appeal 2007-2218
Application 10/035,595
Technology Center 2100

Decided: September 18, 2007

Before: HOWARD B. BLANKENSHIP, ALLEN R. MACDONALD, and COURTENAY, ST. JOHN, III, *Administrative Patent Judges*.

MACDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 from a Final Rejection of claims 1-5 and 7-40. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant invented systems and methods for performing floating point operations, and more particularly systems and methods for performing floating point *addition* with embedded status information associated with a floating point operand. (Spec. [002]).

Representative independent claim 1 under appeal reads as follows:

1. A system for providing a floating point sum, comprising:

> an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and
>
> a results circuit coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the sum of the first floating point operand and the second floating point operand and a resulting status embedded within the resulting floating point operand.

The Examiner rejected claims 1-5 and 7-40 under 35 U.S.C. § 102(b).

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Huang	US 5,995,991	Nov. 30, 1999

The Examiner also rejected claims 1-5 and 7-40 under 35 U.S.C. § 103(a).

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Lynch	US 6,009,511	Dec. 28, 1999

Appellant contends that the claimed subject matter is not disclosed in the prior art. More specifically, Appellant contends Huang fails to disclose a resulting embedded status required by claim 1 because the tag of Huang is separate from the operand. (Reply Br. 6). Appellant also contends that specific features of claims 2-5 are not taught by Huang as alleged by the Examiner. (Reply Br. 7-9). Lastly Appellant contends that Huang fails to teach the limitations of claims 9-14. (Reply Br. 9).

The Examiner contends that in Huang the "resulting status 'tag value' [is] embedded within the 'resulting floating point operand'" (Answer 14), and that the specific features of claims 2-5 and 9-14 are taught by Huang (Answer 5-6).

Further, Appellant contends that the claimed subject matter would not have been obvious. Appellant contends Lynch fails to disclose an embedded status because the tag of Lynch is separate from the operand, and Appellant contends there is no motivation to modify Lynch to yield the claimed invention. (Br. 14-20).

The Examiner contends that it would have been obvious to store the "result with its tag as a resulting operand" to quickly determine its status. (Answer 7).

We affirm.

ISSUE(S)

Has Appellant shown that the Examiner has failed to establish Huang describes "an analyzer circuit" and "a results circuit" as required by claim 1?

Has Appellant shown that the Examiner has failed to establish Huang describes the specific features required by claims 2-5?

Has Appellant shown that the Examiner has failed to establish Huang describes the limitations required by claims 9-14?

Has Appellant shown that the Examiner has failed to establish Lynch suggests "an analyzer circuit" and "a results circuit" as required by claim 1?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Huang

1. The prior art Huang patent describes that "If the generation of the result produces one of a predetermined set of special operands, a tag generator also generates a tag having a predetermined tag value corresponding to the produced special operand." (Col. 5, ll. 43-46).

2. The prior art Huang patent describes that "each of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2." (Col. 6, l. 66 through col. 7, l. 2).

3. Figures 1-3 of Huang show a conventional arithmetic calculation circuit where one or more operands x and y are supplied from a memory device, such as a register file 12 and the operands x and y are inputted to an arithmetic section 14. (Col. 1, ll. 40-42).

4. In the conventional circuit, a zero value result (+ or -) is represented by an operand where (Col. 1, ll. 56-64):

sign= '0' or '1' bit,

exponent=a sequence of eight '0' bits,

magnitude=a sequence of twenty-three '0' bits.

5. In the conventional circuit, when the arithmetic section 14 performs an operation that results in a value other than an ordinary operand value, the arithmetic unit outputs a signal indicating that the result is zero, infinity or not a number to the generator circuit 22. In response, the circuit 22 generates the appropriate output floating point number as per the IEEE standard of special operands set. (Col. 2, ll. 55-59).

6. In the conventional circuit, interposed between the register file and the arithmetic section 14 are detectors 24 and 26. One detector 24 or 26 is provided for each operand input path. The detectors 24 and 26 each receive a respective operand x or y and determines whether or not the received operand represents a special operand. If not, the detector 24 or 26 simply outputs the operand x or y to the arithmetic section 14. However, if the detector 24 or 26 detects that the operand x or y represents a special operand, the detector 24 or 26 identifies the type of the operand--the detector determines which of the special operands the received operand x or y represents. (Col. 3, ll. 11-21).

7. FIG. 2 shows an exemplary special operand generator circuit 22 in greater detail. As shown, the special operand generator circuit 22 includes first and second multiplexers 222 and 224.

8. In the conventional circuit, the arithmetic section 14 outputs appropriate selector control signals to the multiplexer 222 to output a resulting exponent, and to the multiplexer 224 to output a resulting magnitude of an arithmetic operation. (Col. 3, ll. 42-45 and 60-63).

9. In the conventional circuit, when the result of an arithmetic operation is zero, the arithmetic section outputs selector control signals to the multiplexers 222 and 224 for selecting the eight '0' bits for the exponent and twenty-three '0' bits for the magnitude. (col. 3, ll. 66-67, and col. 4, ll. 1-4).

10. FIG. 3 shows a conventional detector 24 or 26. As shown, the detector 24 or 26 includes two comparator circuits 252 and 254. (Col. 4, ll. 24-26).

11. In the conventional circuit, three AND gates 261, 262 and 263 are also provided. The AND gate 261 receives as inputs the logic bits outputted on the lines 255 and 257. The AND gate 261 therefore outputs a signal indicating whether or not the operand represents a zero valued special operand. (Col. 4, ll. 41-45).

12. The prior art Lynch patent describes that the "FPU [floating point unit] core uses the tag value associated with an operand to determine whether the tag value is a special floating point number." (Col. 16, ll. 62-65).

PRINCIPLES OF LAW

On appeal, Appellant bears the burden of showing that the Examiner has not established a legally sufficient basis for anticipation based on the Huang patent.

Appellant may sustain this burden by showing that the prior art reference relied upon by the Examiner fails to disclose an element of the claim. It is axiomatic that anticipation of a claim under § 102 can be found

only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). *See also KSR*, 127 S. Ct. at 1734, 82 USPQ2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR.*, 127 S. Ct. at 1741 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

Claim Interpretation

Claim 1 recites an analyzer circuit configured to determine a first status and a second status based on data within respective first and second floating point operands.

Claim 1 further recites a results circuit coupled to the analyzer circuit and configured to "assert a resulting floating point operand containing the sum of the first floating point operand and the second floating point operand and a resulting status embedded within the resulting floating point operand."

We interpret claim 1 as requiring at least: 1) a plurality of operands each of which "containing" encoded status flag information, and 2) a result circuit that produces a resulting floating point operand containing both a sum (a result value) and status information.

The language of claim 1 does not preclude the sum and the status information from being represented by the same data within the resulting floating point operand. See FF 4 above for an example of a floating point operand whose bits result in a value of "zero" and whose bit string has been assigned a status of representing "zero."[1]

As to claims 9-14, these claims fail to recite any structural or functional limitations. Rather, each of these claims merely indicate the

[1] We note that claim 1 would distinguish over the cited prior art if the claim were amended to require a single resulting floating point operand that contains distinct parts which represent a value and encoded status information.

numerical value of the operand (claims 10 and 12) or indicates what the data within the operand will represent (claims 9, 11, 13, and 14).

35 U.S.C. § 102

Appellant correctly points out that the device of figure 4 of Huang does not produce "a resulting floating point operand containing the sum of the first floating point operand and the second floating point operand and a resulting status embedded within the resulting floating point operand" as required by claim 1. Contrary to the Examiner's contention (Answer 14), Huang's "tag value" does not "constitute a teaching [of] data within the floating point operand as claimed." Rather, Huang discloses that the tag (status info) stands separate from the operand (result). (FF 1 and 2).

However, Prior Art figures 1-3 of Huang teach all the features of claims 1-5. See FF 3-11. Claim 1 – an analyzer circuit (items 24 & 26) and a results circuit (items 14 & 22). Claim 2 – a first buffer (inherent to item 24 which receives and outputs), a second buffer (similarly inherent to item 26), first operand analysis circuit (items 252, 254, & 261 of item 24), and second operand analysis circuit (items 252, 254, & 261 of item 26). Claims 3 and 4 – memory storage (item 12). Claim 5 – an adder circuit (item 14, see FF 8), an adder logic circuit (item 14, see FF 9), and a result assembler (item 22).

For the special case of addition of the "zero" operand plus the "zero" operand to yield the "zero" operand, the conventional circuit corresponds to the subject matter of Appellant's claims 1-5. Thus, contrary to Appellant's ultimate contention, Huang does disclose the subject matter of claims 1-5.

Therefore, Appellant has not established that the Examiner erred with respect to this contention.

As to claims 9-14, Appellant fails to point out any structural or functional limitation that distinguishes these claims over the prior art. As we noted in the claim interpretation above, no such limitations exist. Therefore, Appellant has not established that the Examiner erred with respect to the rejection of these claims.

Since Appellant has not separately argued the remaining rejected claims, they stand or fall with claim 1 or the claims from which they depend.

35 U.S.C. § 103

The Lynch patent parallels the Huang patent in that both append a status tag to a floating point operand to improve on the conventional method of handling special status operands. As above with Huang, Appellant correctly points out that the appended tags of Lynch do not correspond with the limitations of claim 1. However, also as above with Huang, the conventional background art of Lynch (cols. 1 and 2) does correspond to the subject matter of claim 1.

Lynch's background art disclosure differs from Huang in that Lynch describes the functions to be performed (encoding, determining special encoding, decoding, etc.) and fails to explicitly disclose specific structures for performing the disclosed background art functions. However, Lynch also specifically discloses that "logic circuits" comprise his instruction processing pipeline invention. See Lynch's figures 1-4. We conclude that the level of skill in the art as demonstrated by Lynch is sufficient that one

skilled in the art would recognize that the background art functions could be implemented with logic circuits similar to those used by Lynch to implement his invention. Thus, the subject matter of claim 1 is obvious over the combination of disclosures in Lynch.

Appellant has not established that the Examiner erred with respect to the rejection of claim 1. Since Appellant has not separately argued the remaining rejected claims, they stand or fall with claim 1.

NEW GROUNDS OF REJECTION

Our decision relies on different reasoning than that set forth by the Examiner. Due to our new reasoning, we designate our decision as a new ground of rejection.

37 C.F.R. § 41.50(b)

37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ...
>
> (2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record ...

CONCLUSION OF LAW

(1) Appellant has not established that the Examiner erred in rejecting claims 1-5 and 7-40 as being unpatentable under 35 U.S.C. § 102(b) over Huang.

(2) Appellant has not established that the Examiner erred in rejecting claims 1-5 and 7-40 as being unpatentable under 35 U.S.C. § 103(a) over Lynch.

(3) Claims 1-5 and 7-40 are not patentable.

DECISION

The Examiner's rejection of claims 1-5 and 7-40 is Affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED
37 C.F.R. § 41.50(b)

pgc

SUN MICROSYSTEMS/FINNEGAN, HENDERSON LLP
901 NEW YORK AVENUE, NW
WASHINGTON DC 20001-4413